

DATA SHEET

TDA8561Q

**2 x 24 W BTL or 4 x 12 W
single-ended car radio power
amplifier**

Preliminary specification
File under Integrated Circuits, IC01

July 1994

2 x 24 W BTL or 4 x 12 W single-ended car radio power amplifier

TDA8561Q

FEATURES

- Requires very few external components
- High output power
- Flexibility in use - Quad single-ended or stereo BTL
- Low output offset voltage
- Fixed gain
- Diagnostic facility (distortion, short-circuit and temperature detection)
- Good ripple rejection
- Mode select switch (operating, mute and stand-by)
- Load dump protection
- AC and DC short-circuit safe to ground and to V_P
- Low power dissipation in any short-circuit condition
- Thermally protected

- Reverse polarity safe
- Electrostatic discharge protection
- No switch-on/switch-off pop
- Flexible leads
- Low thermal resistance
- Identical inputs (inverting and non-inverting).

GENERAL DESCRIPTION

The TDA8561Q is an integrated class-B output amplifier in a 17-lead single-in-line (SIL) power package. It contains 4 x 12 W single-ended or 2 x 24 W bridge amplifiers.

The device is primarily developed for car radio applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive operating supply voltage		6	14.4	18	V
I_{ORM}	repetitive peak output current		–	–	4	A
I_P	total quiescent current		–	80	–	mA
I_{sb}	stand-by current		–	0.1	100	μ A
Stereo BTL application						
P_O	output power	4 Ω ; THD = 10%	–	24	–	W
RR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	$R_s = 0 \Omega$	–	70	–	μ V
$ Z_I $	input impedance		25	–	–	k Ω
$ \Delta V_{O} $	DC output offset voltage		–	–	150	mV
Quad single-ended application						
P_O	output power	THD = 10%				
		4 Ω	–	7	–	W
		2 Ω	–	12	–	W
RR	supply voltage ripple rejection		48	–	–	dB
V_{no}	noise output voltage	$R_s = 0 \Omega$	–	50	–	μ V
$ Z_I $	input impedance		50	–	–	k Ω

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ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8561Q	17	DBS	plastic	SOT243R ⁽¹⁾

Note

1. SOT243-1; 1996 August 30.

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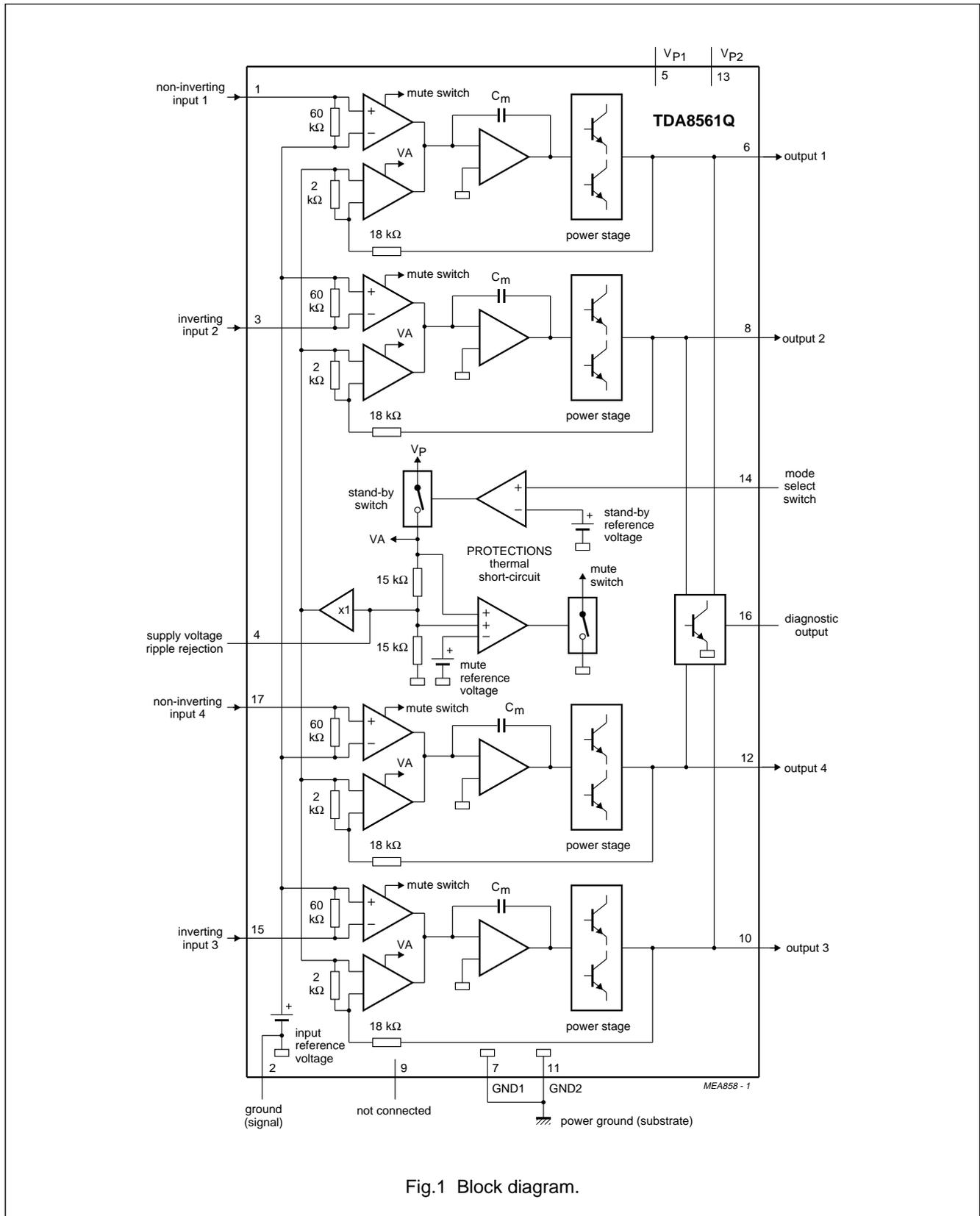


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
-INV 1	1	non-inverting input 1
GND(S)	2	signal ground
INV 2	3	inverting input 2
RR	4	supply voltage ripple rejection
V _{P1}	5	supply voltage
OUT 1	6	output 1
GND1	7	power ground 1
OUT 2	8	output 2
n.c.	9	not connected
OUT 3	10	output 3
GND2	11	power ground 2
OUT 4	12	output 4
V _{P2}	13	supply voltage
MODE	14	mode select switch input
INV 3	15	inverting input 3
V _{DIAG}	16	diagnostic output
-INV 4	17	non-inverting input 4

FUNCTIONAL DESCRIPTION

The TDA8561Q contains four identical amplifiers and can be used for single-ended or bridge applications. The gain of each amplifier is fixed at 20 dB (26 dB in BTL). Special features of the device are:

Mode select switch (pin 14)

- low stand-by current (< 100 μA)
- low switching current (low cost supply switch)
- mute facility

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during ≥ 100 ms (charging of the input capacitors at pin 1, 3, 15 and pin 17).

This can be achieved by:

- microprocessor control
- external timing circuit (see Fig.11)

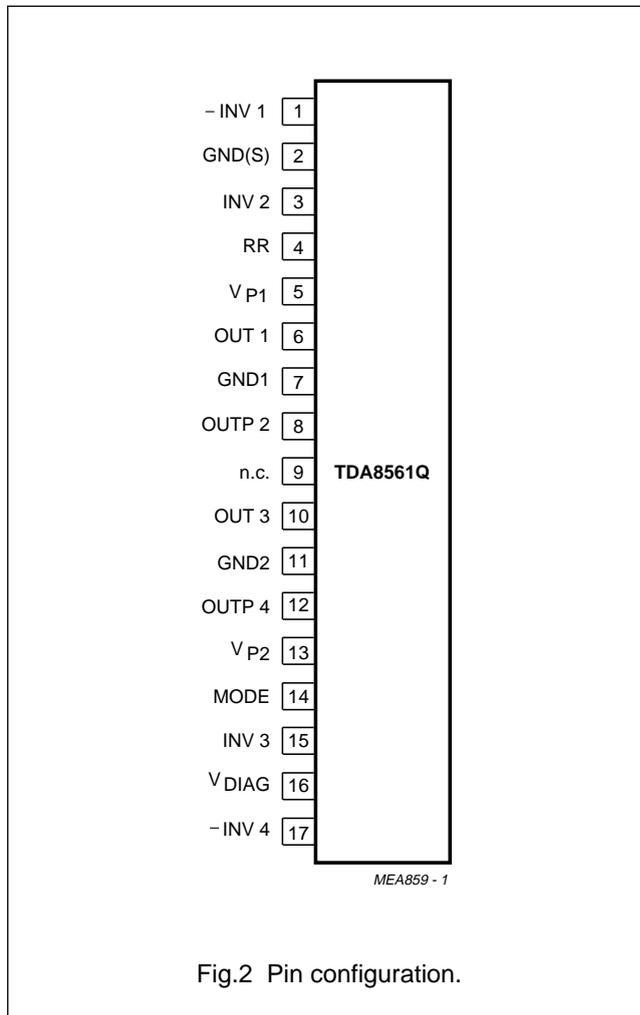


Fig.2 Pin configuration.

Diagnostic output (pin 16)

DYNAMIC DISTORTION DETECTOR (DDD)

At the onset of clipping of one or more output stages, the dynamic distortion detector becomes active and pin 16 goes low. This information can be used to drive a sound processor or DC volume control to attenuate the input signal and thus limit the distortion. The output level of pin 16 is independent of the number of channels that are clipping (see Fig.3 and Fig.4).

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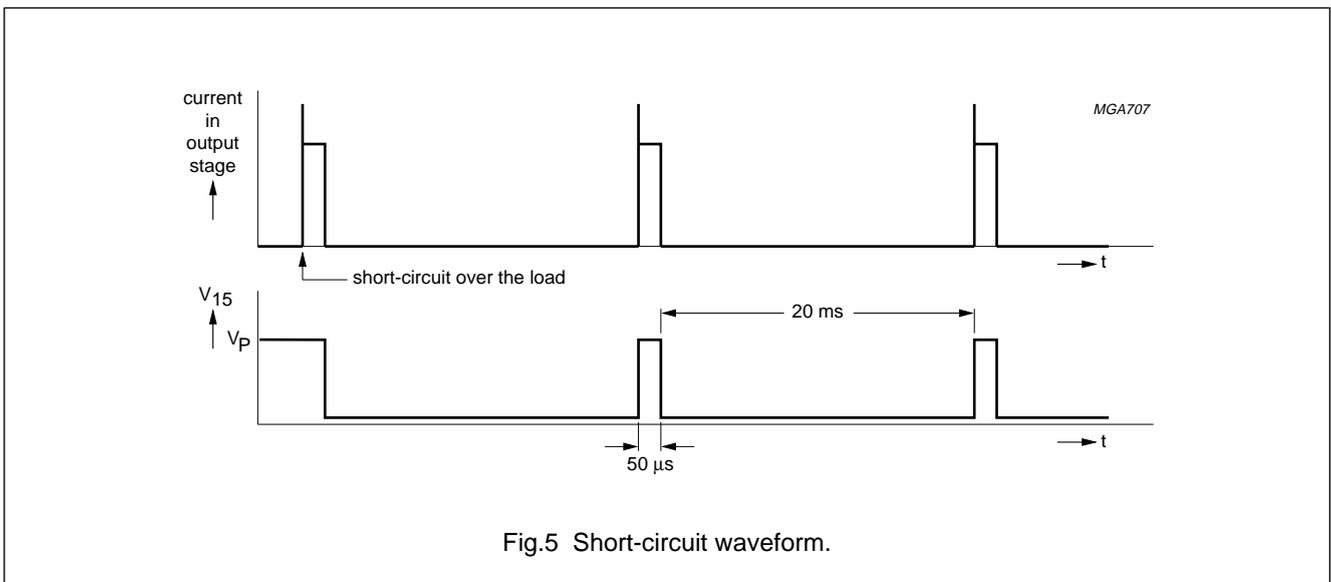
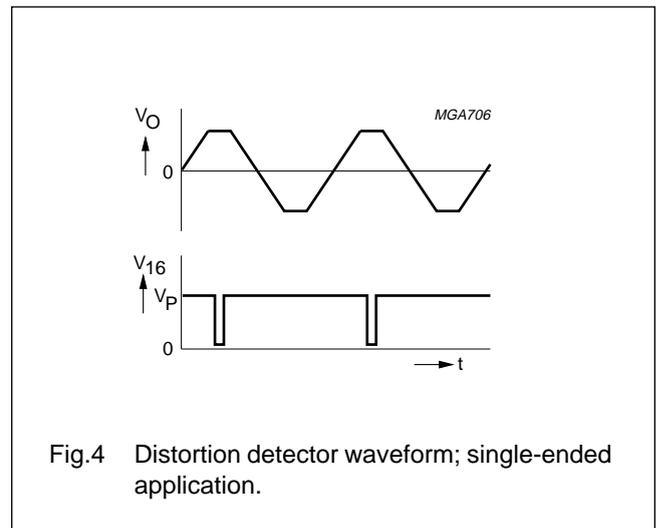
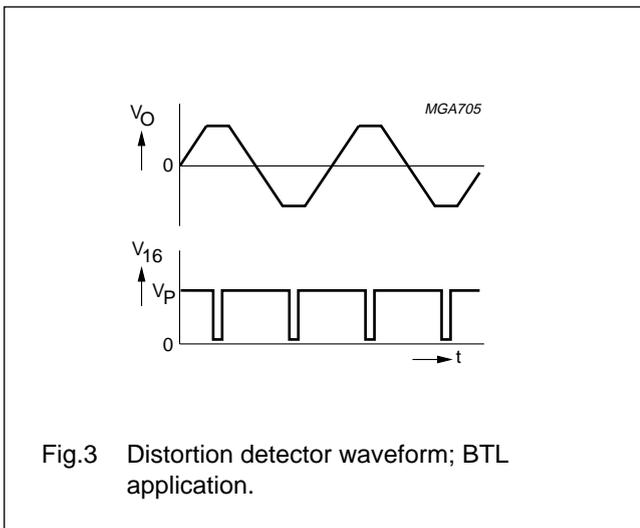
SHORT-CIRCUIT PROTECTION

When a short-circuit occurs at one or more outputs to ground or to the supply voltage, the output stages are switched off until the short-circuit is removed and the device is switched on again, with a delay of approximately 20 ms, after removal of the short-circuit. During this short-circuit condition, pin 16 is continuously low.

When a short-circuit across the load of one or both channels occurs the output stages are switched off during approximately 20 ms. After that time it is checked during approximately 50 μ s to see whether the short-circuit is still present. Due to this duty cycle of 50 μ s/20 ms the average current consumption during this short-circuit condition is very low (approximately 40 mA).

During this short-circuit condition, pin 16 is low for 20 ms and high for 50 μ s (see Fig.5).

The power dissipation in any short-circuit condition is very low.



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TEMPERATURE DETECTION

When the virtual junction temperature T_{vj} reaches 150 °C, pin 16 will be active LOW.

OPEN COLLECTOR OUTPUT

Pin 16 is an open collector output, which allows pin 16 of more devices being tied together.

LIMITING VALUES

In accordance with the absolute maximum system (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_p	positive supply voltage		–	18	V
	operating		–	30	V
	non-operating		–	45	V
	load dump protection	during 50 ms; $t_r \geq 2.5$ ms	–	45	V
I_{OSM}	non-repetitive peak output current		–	6	A
I_{ORM}	repetitive peak output current		–	4	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
T_{vj}	virtual junction temperature		–	150	°C
V_{psc}	AC and DC short-circuit safe voltage		–	18	V
V_{pr}	reverse polarity		–	6	V
P_{tot}	total power dissipation		–	60	W

THERMAL RESISTANCE

In accordance with IEC 747-1.

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	40 K/W
$R_{th\ j-c}$	from junction to case (see Fig.6 and Fig.7)	1.3 K/W

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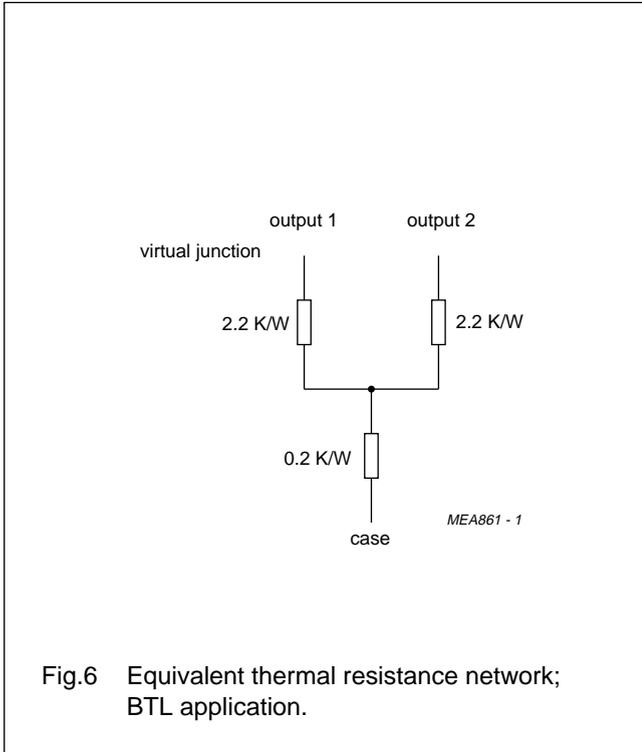


Fig.6 Equivalent thermal resistance network;
BTL application.

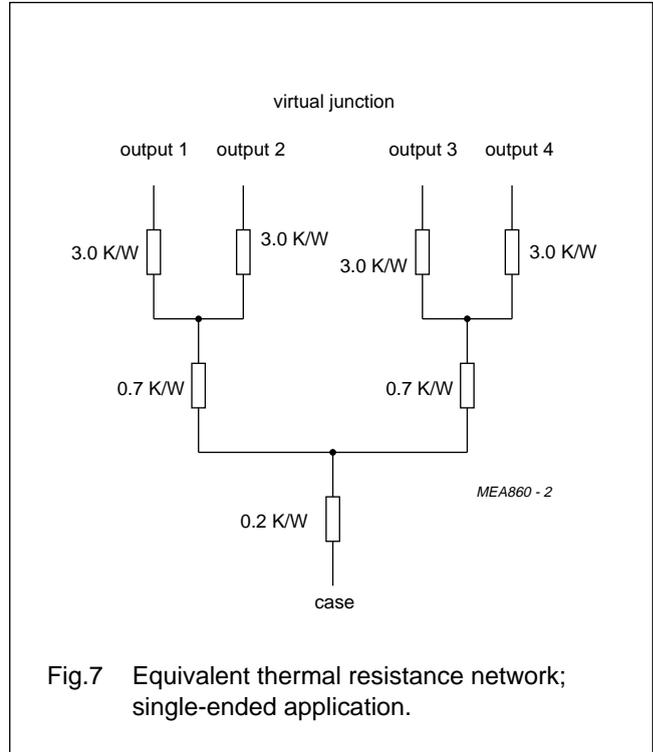


Fig.7 Equivalent thermal resistance network;
single-ended application.

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DC CHARACTERISTICS

$V_P = 14.4$ V; $T_{amb} = 25$ °C; measured in Fig.8; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	positive supply voltage	note 1	6	14.4	18	V
I_P	quiescent current		–	80	160	mA
V_O	DC output voltage	note 2	–	6.9	–	V
$ \Delta V_O $	DC output offset voltage		–	–	150	mV
Mode select switch						
V_{on}	switch-on voltage level		8.5	–	–	V
MUTE CONDITION						
V_{mute}	mute voltage		3.3	–	6.4	V
V_O	output voltage in mute position	$V_{Imax} = 1$ V; $f = 1$ kHz	–	–	2	mV
$ \Delta V_O $	DC output offset voltage (between pins 6-8 and 10-12)		–	–	150	mV
STAND-BY CONDITION						
V_{sb}	stand-by voltage		0	–	2	V
I_{sb}	stand-by current		–	–	100	μ A
I_{sw}	switch-on current		–	12	40	μ A
Diagnostic output (pin 16)						
V_{DIAG}	diagnostic output voltage	any short-circuit or clipping	–	–	0.6	V

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AC CHARACTERISTICS

$V_P = 14.4$ V; $R_L = 4$ Ω ; $f = 1$ kHz; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Stereo BTL application (measured in Fig.8)						
P_O	output power	note 7				
		THD = 0.5%	15	19	–	W
		THD = 10%	20	24	–	W
THD	total harmonic distortion	$P_O = 1$ W	–	0.1	–	%
P_O	output power	$V_P = 13.2$ V				
		THD = 0.5%	–	16	–	W
		THD = 10%	–	20	–	W
B	power bandwidth	THD = 0.5%; $P_O = -1$ dB; with respect to 15 W	–	20 to 15000	–	Hz
f_l	low frequency roll-off	at -1 dB; note 3	–	45	–	Hz
f_h	high frequency roll-off	at -1 dB	20	–	–	kHz
G_v	closed loop voltage gain		25	26	27	dB
RR	supply voltage ripple rejection	note 4				
	on		48	–	–	dB
	mute		48	–	–	dB
	stand-by		80	–	–	dB
$ Z_i $	input impedance		25	30	38	k Ω
V_{no}	noise output voltage					
	on	$R_s = 0$ Ω ; note 5	–	70	–	μ V
	on	$R_s = 10$ k Ω ; note 5	–	100	200	μ V
	mute	notes 5 and 6	–	60	–	μ V
α	channel separation	$R_s = 10$ k Ω	40	–	–	dB
$ \Delta G_v $	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	$V_{16} \leq 0.6$ V; no short-circuit	–	10	–	%
Quad single-ended application (measured in Fig.9)						
P_O	output power	note 7				
		THD = 0.5%	4	5	–	W
		THD = 10%	5.5	7	–	W
THD	total harmonic distortion	$P_O = 1$ W	–	0.1	–	%
P_O	output power	$R_L = 2$ Ω ; note 7				
		THD = 0.5%	7.5	10	–	W
		THD = 10%	10	12	–	W
f_l	low frequency roll-off	at -3 dB; note 3	–	45	–	Hz
f_h	high frequency roll-off	at -1 dB	20	–	–	kHz
G_v	closed loop voltage gain		19	20	21	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RR	supply voltage ripple rejection	note 4				
	on		48	–	–	dB
	mute		48	–	–	dB
	stand-by		80	–	–	dB
$ Z_i $	input impedance		50	60	75	k Ω
V_{no}	noise output voltage					
	on	$R_s = 0 \Omega$; note 5	–	50	–	μ V
	on	$R_s = 10 \text{ k}\Omega$; note 5	–	70	100	μ V
	mute	notes 5 and 6	–	50	–	μ V
α	channel separation	$R_s = 10 \text{ k}\Omega$	40	–	–	dB
$ \Delta G_v $	channel unbalance		–	–	1	dB
DYNAMIC DISTORTION DETECTOR						
THD	total harmonic distortion	$V_{16} \leq 0.6 \text{ V}$; no short-circuit	–	10	–	%

Notes

1. The circuit is DC adjusted at $V_P = 6$ to 18 V and AC operating at $V_P = 8.5$ to 18 V.
2. At $18 \text{ V} < V_P < 30 \text{ V}$ the DC output voltage $\leq V_P/2$.
3. Frequency response externally fixed.
4. Ripple rejection measured at the output with a source impedance of 0Ω , maximum ripple amplitude of 2 V (p-p) and at a frequency of between 100 Hz and 10 kHz.
5. Noise measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_s ($V_i = 0 \text{ V}$).
7. Output power is measured directly at the output pins of the IC.

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TEST/APPLICATION INFORMATION

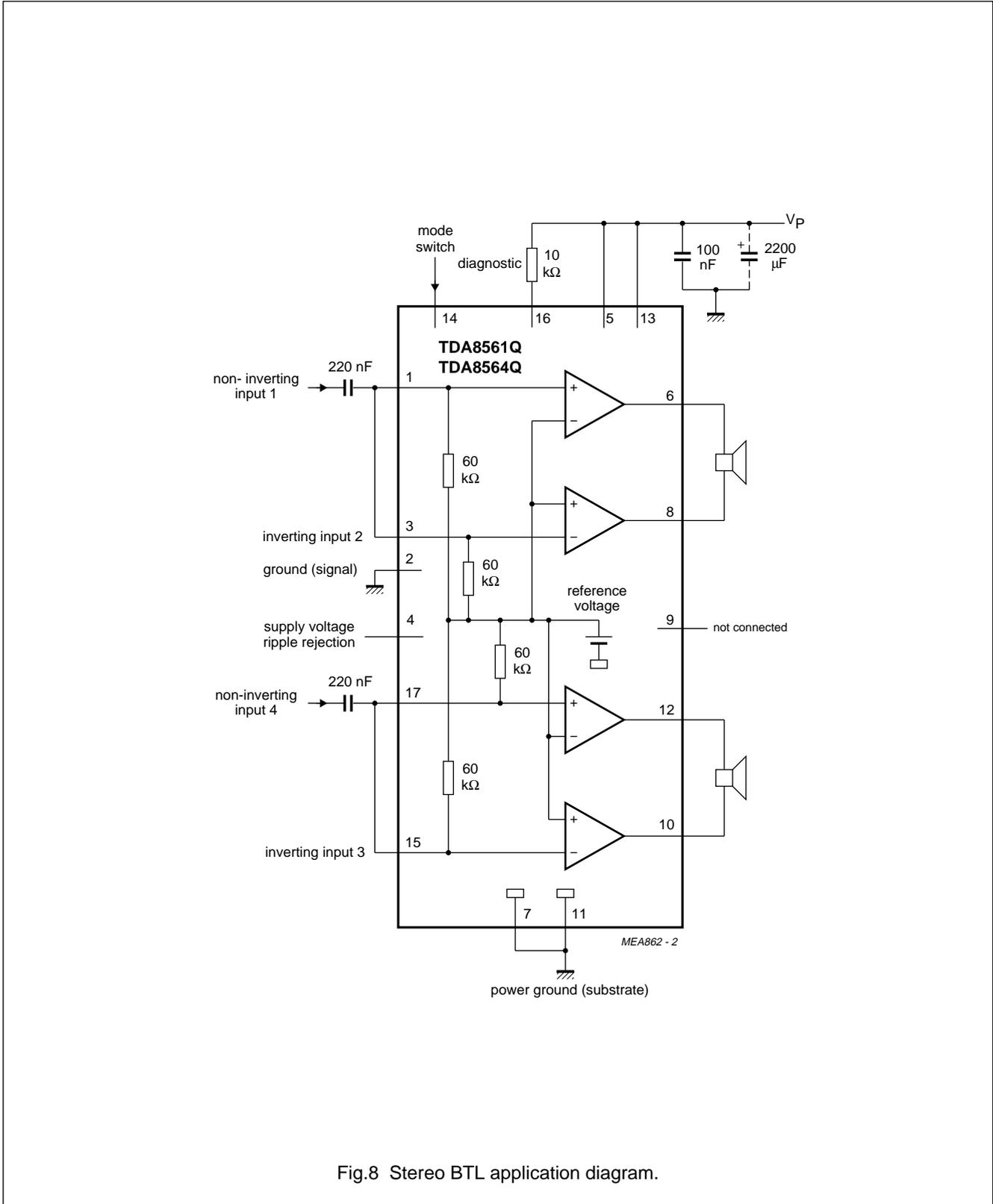


Fig.8 Stereo BTL application diagram.

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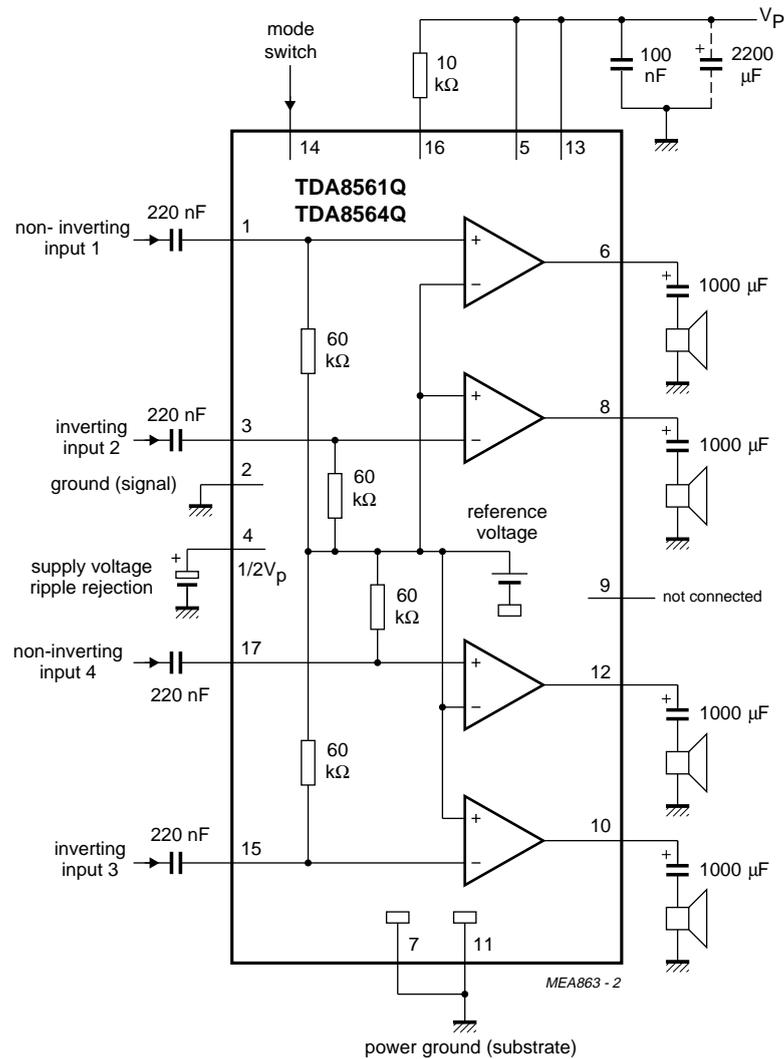
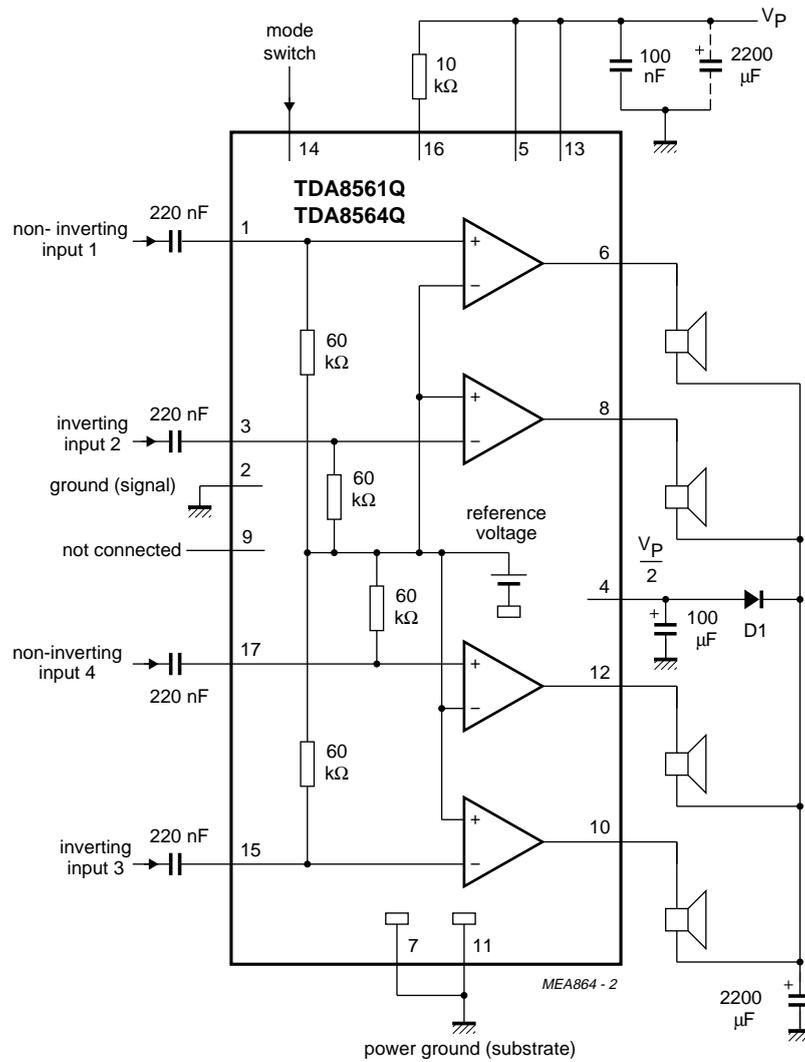


Fig.9 Quad single-ended application diagram 1.

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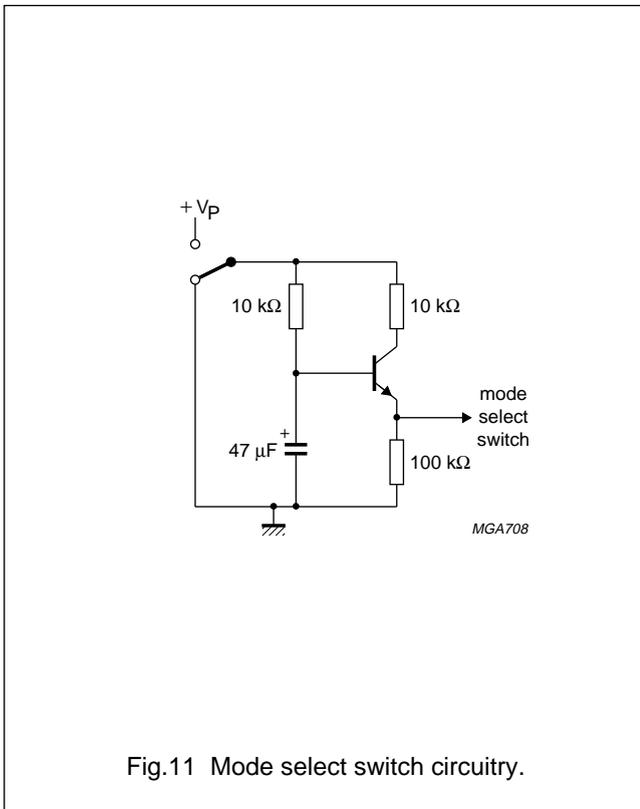


(1) When short-circuiting the single-ended capacitor, the dissipation will be reduced due to diode D1.

Fig.10 Quad single-ended application diagram 2.

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Mode select switch

To avoid switch-on plops, it is advised to keep the amplifier in the mute mode during > 100 ms (charging of the input capacitors at pins 1, 3, 15 and 17).

The circuit in Fig.11 slowly ramps up the voltage at the mode select switch pin when switching on and results in fast muting when switching off.

Fig.11 Mode select switch circuitry.

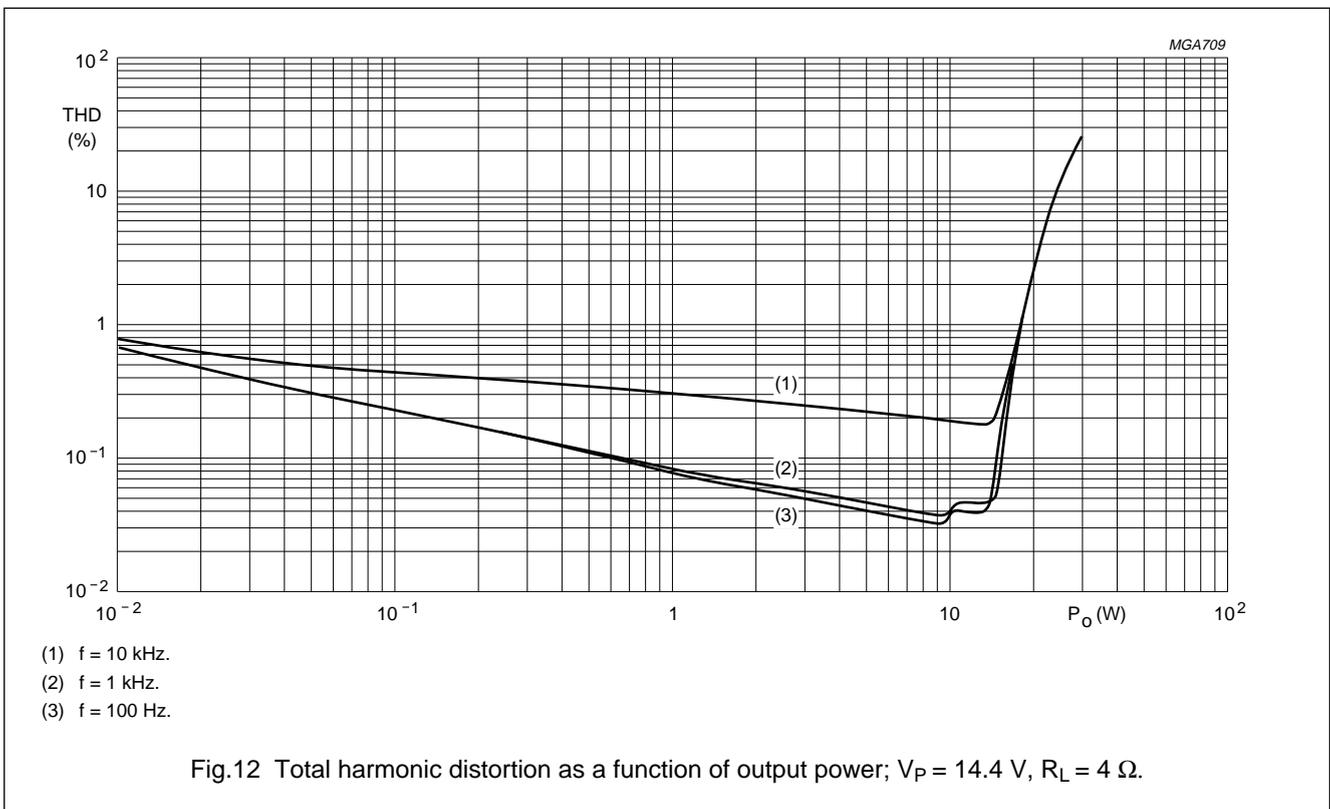
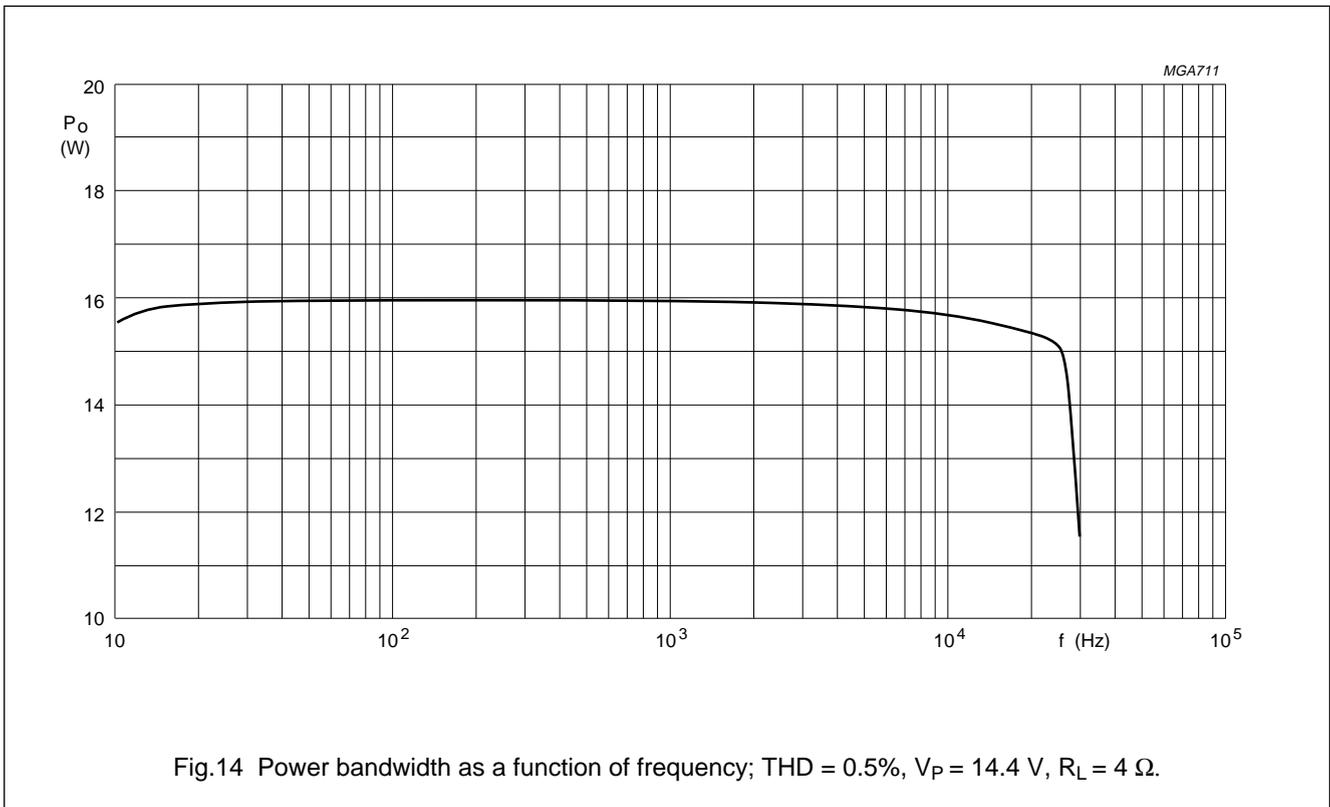
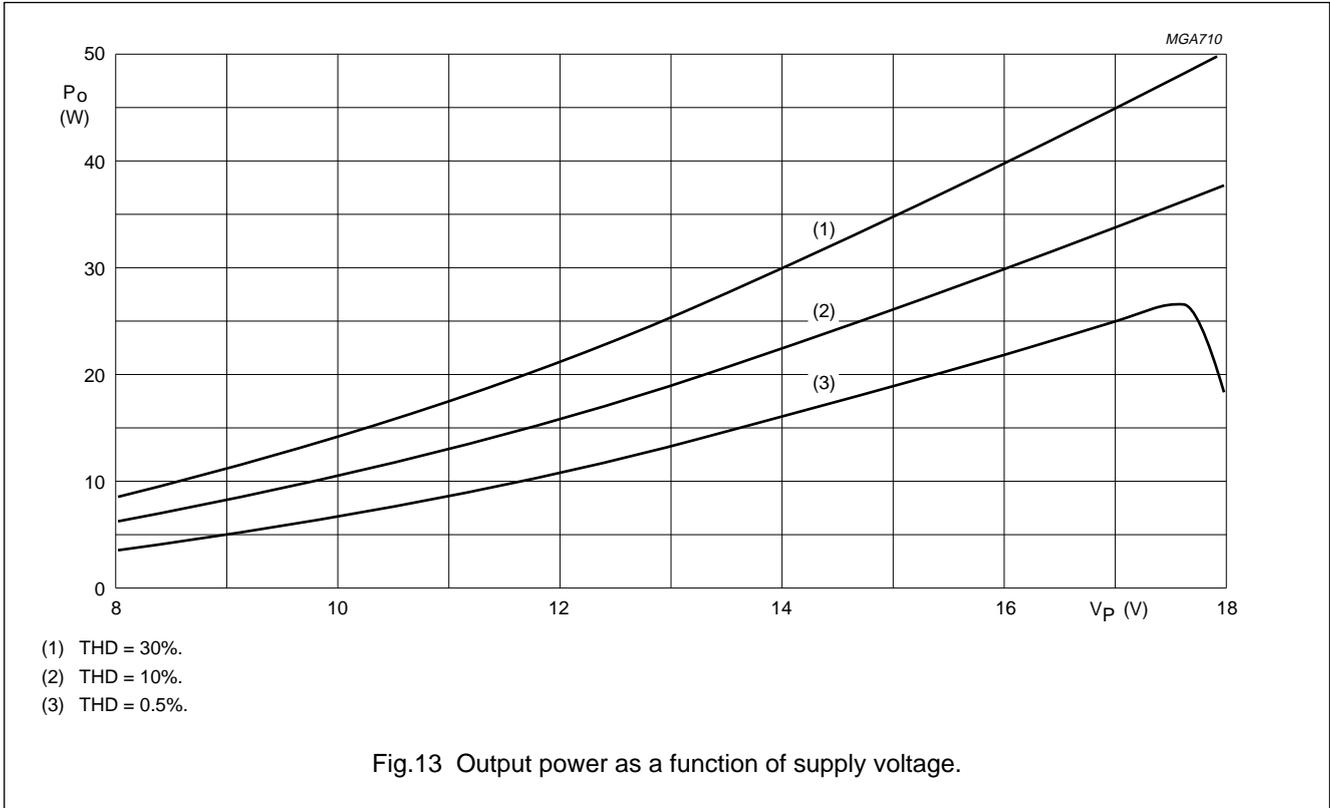


Fig.12 Total harmonic distortion as a function of output power; $V_P = 14.4 \text{ V}$, $R_L = 4 \Omega$.

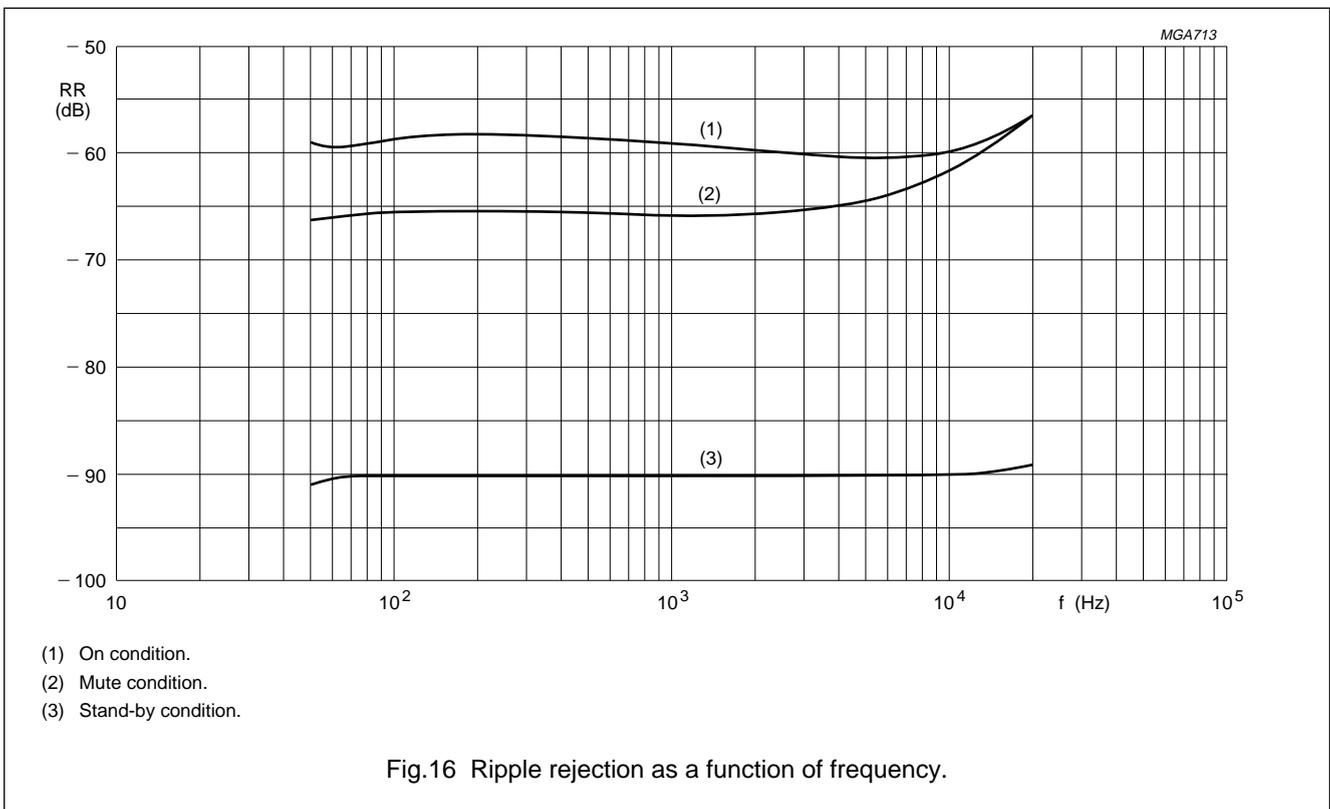
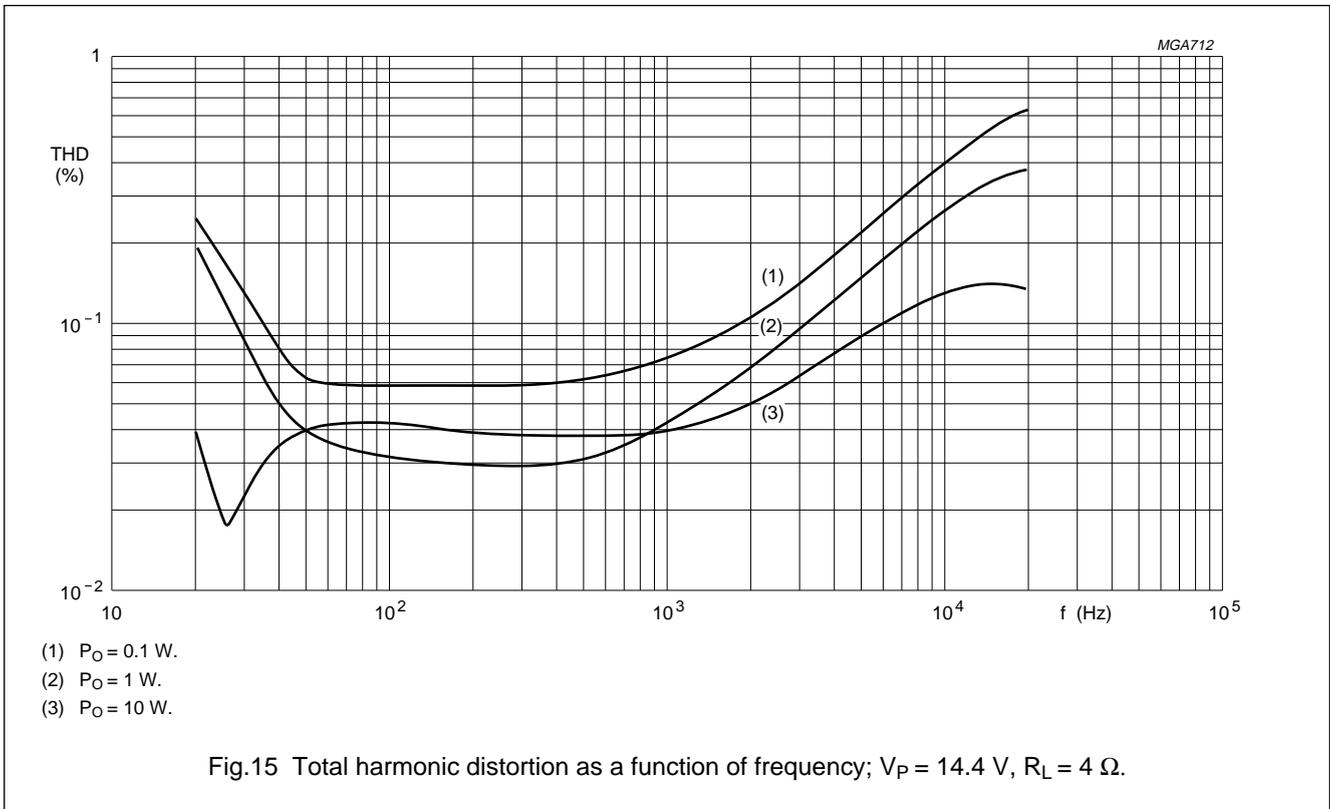
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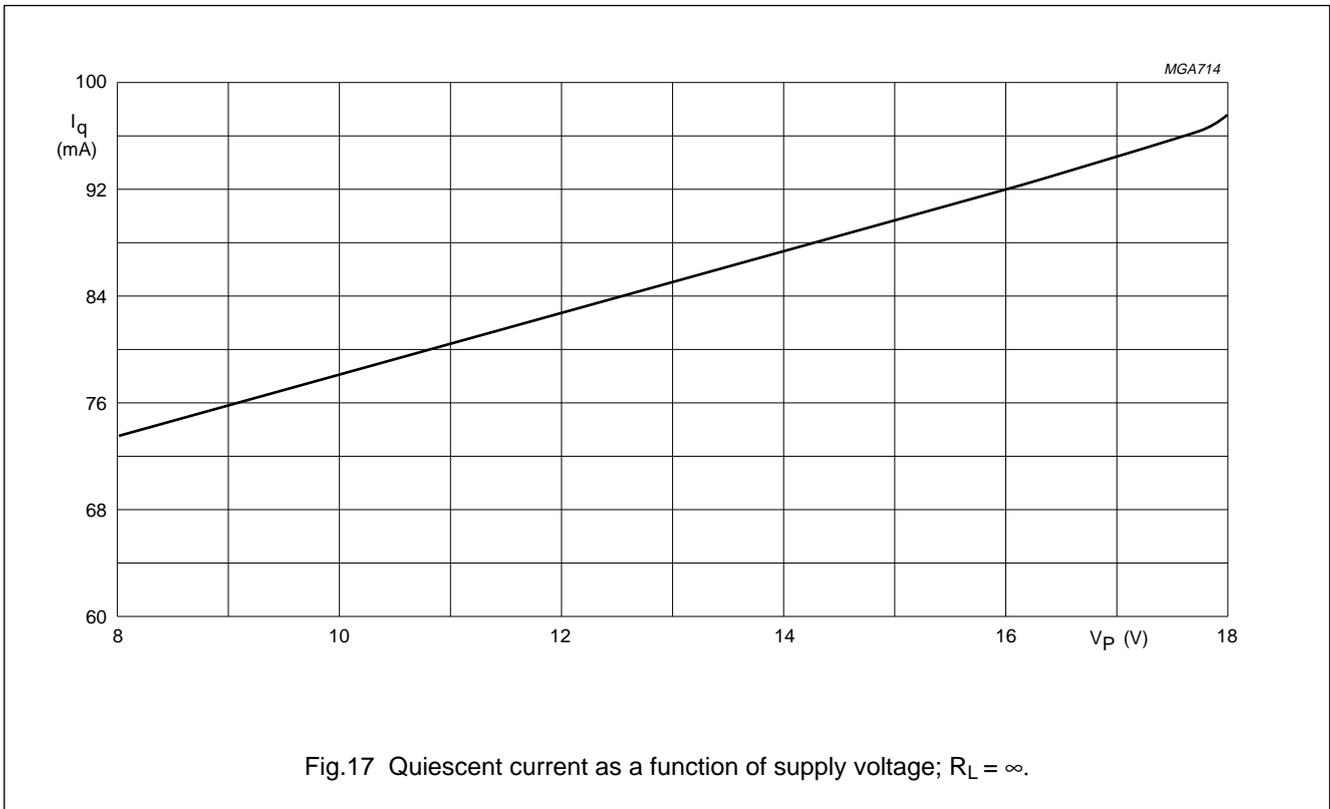
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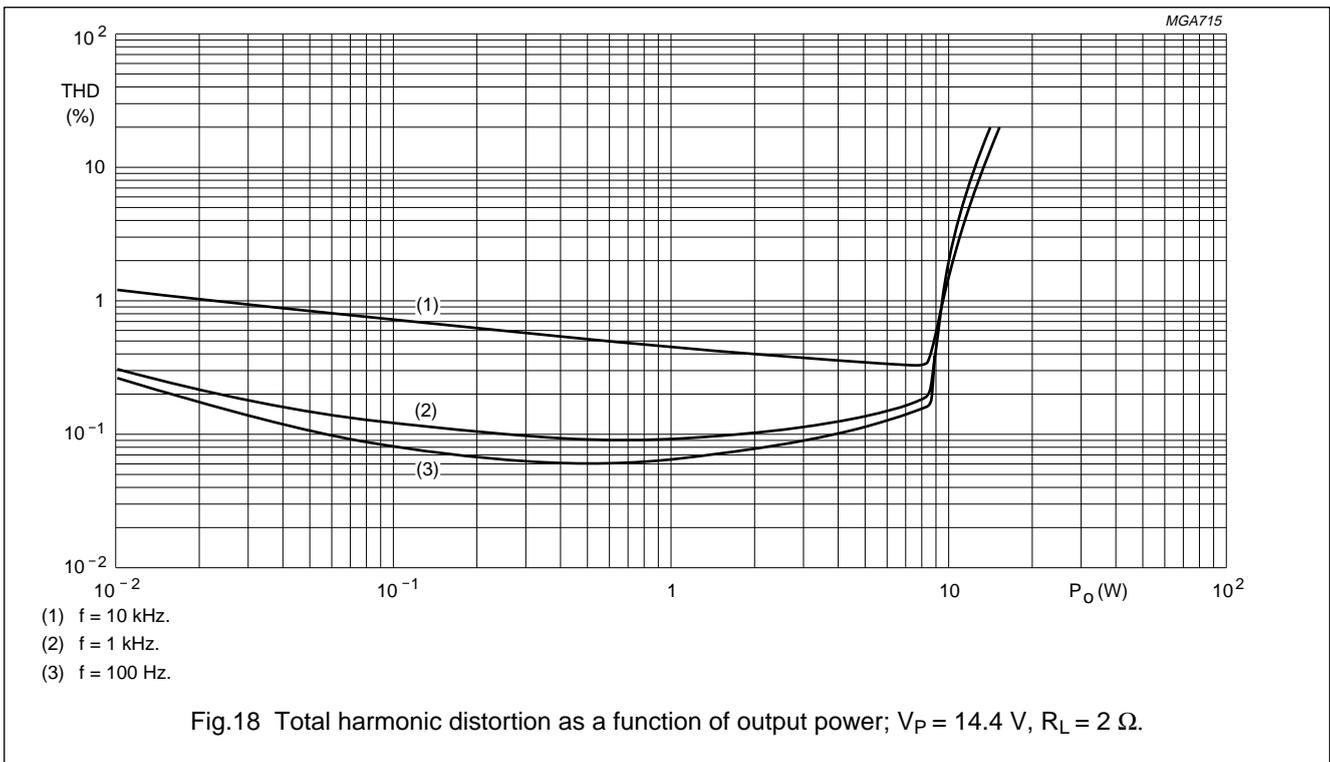


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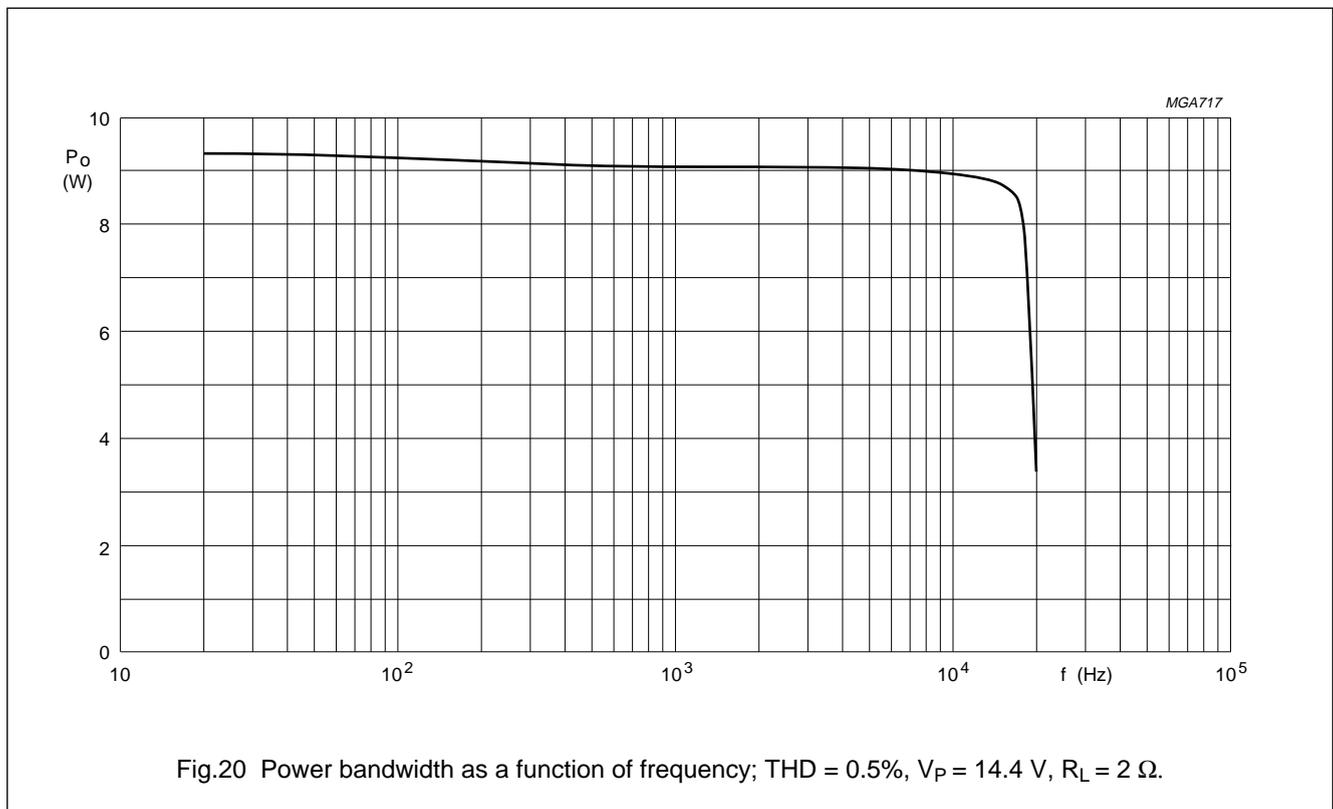
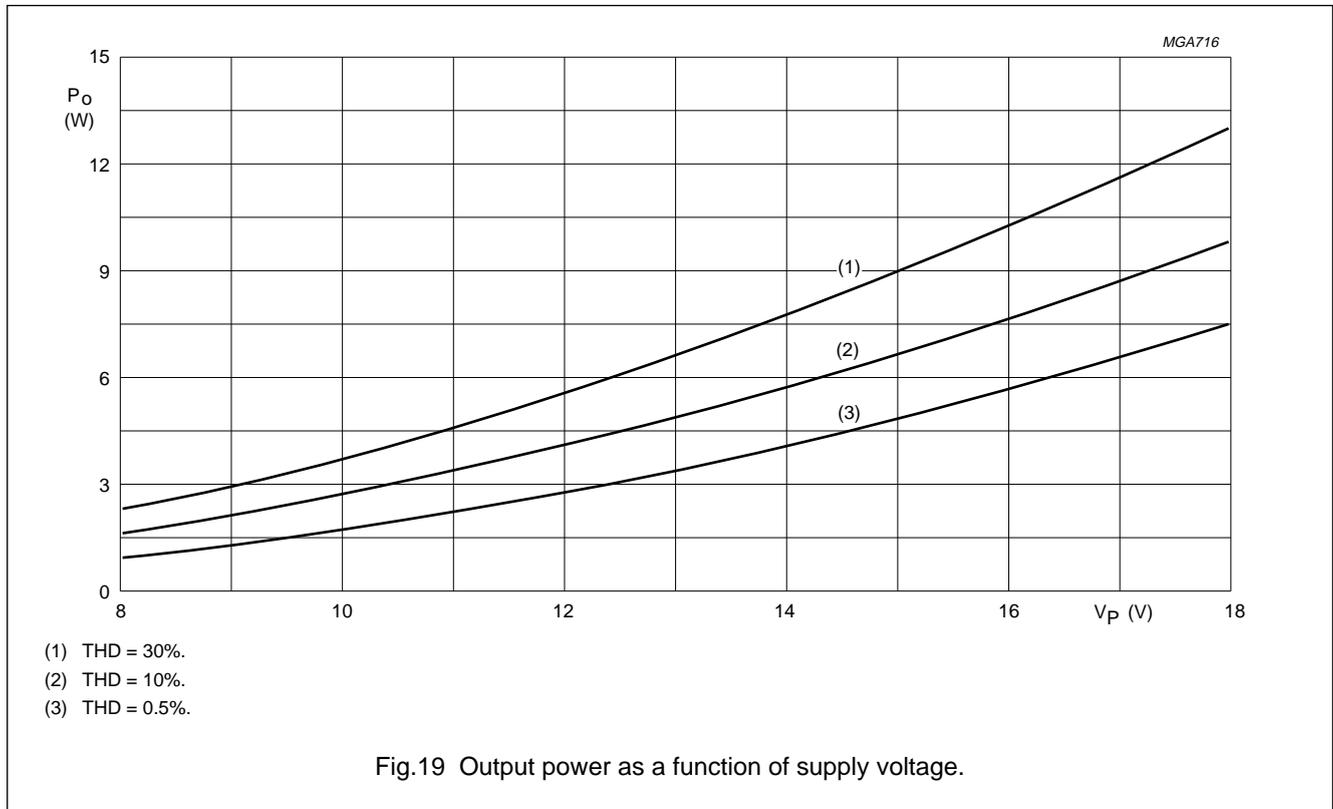


SINGLE-ENDED APPLICATION



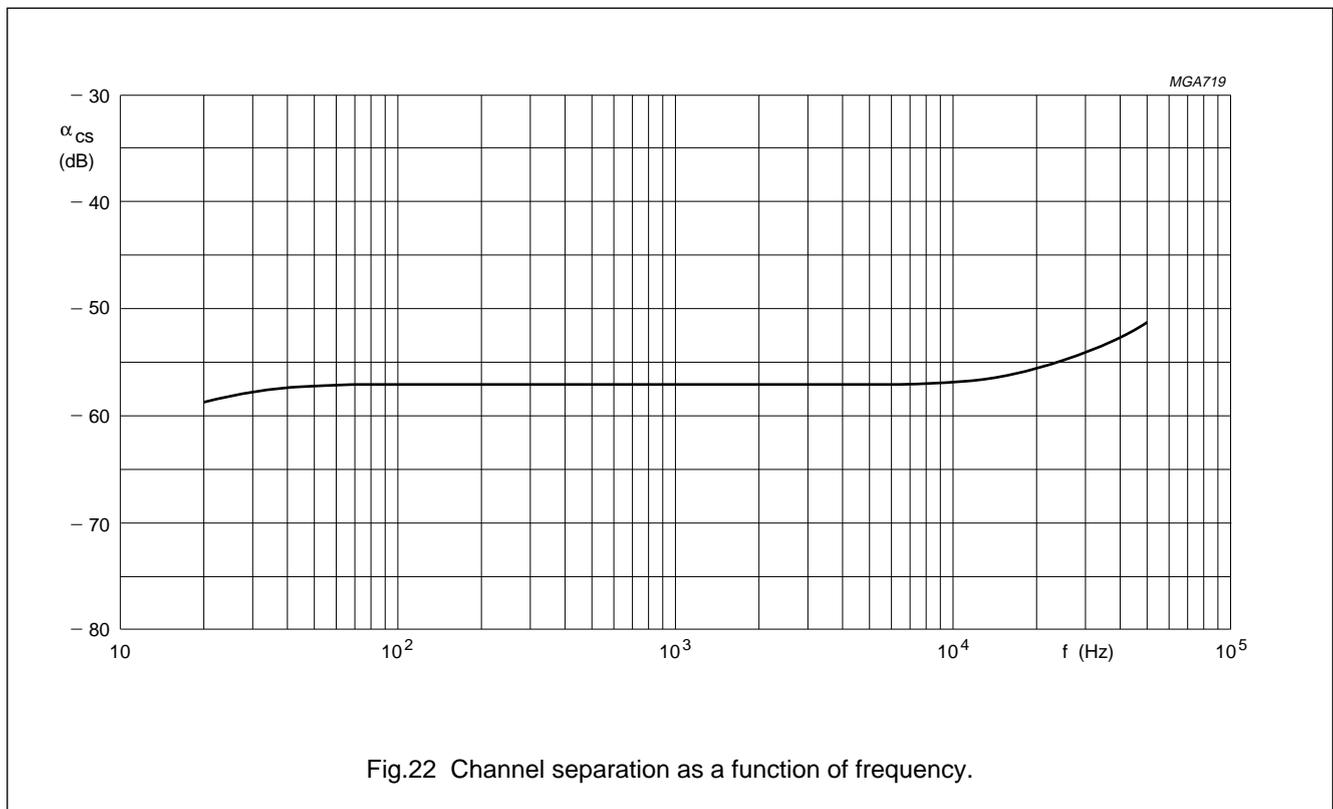
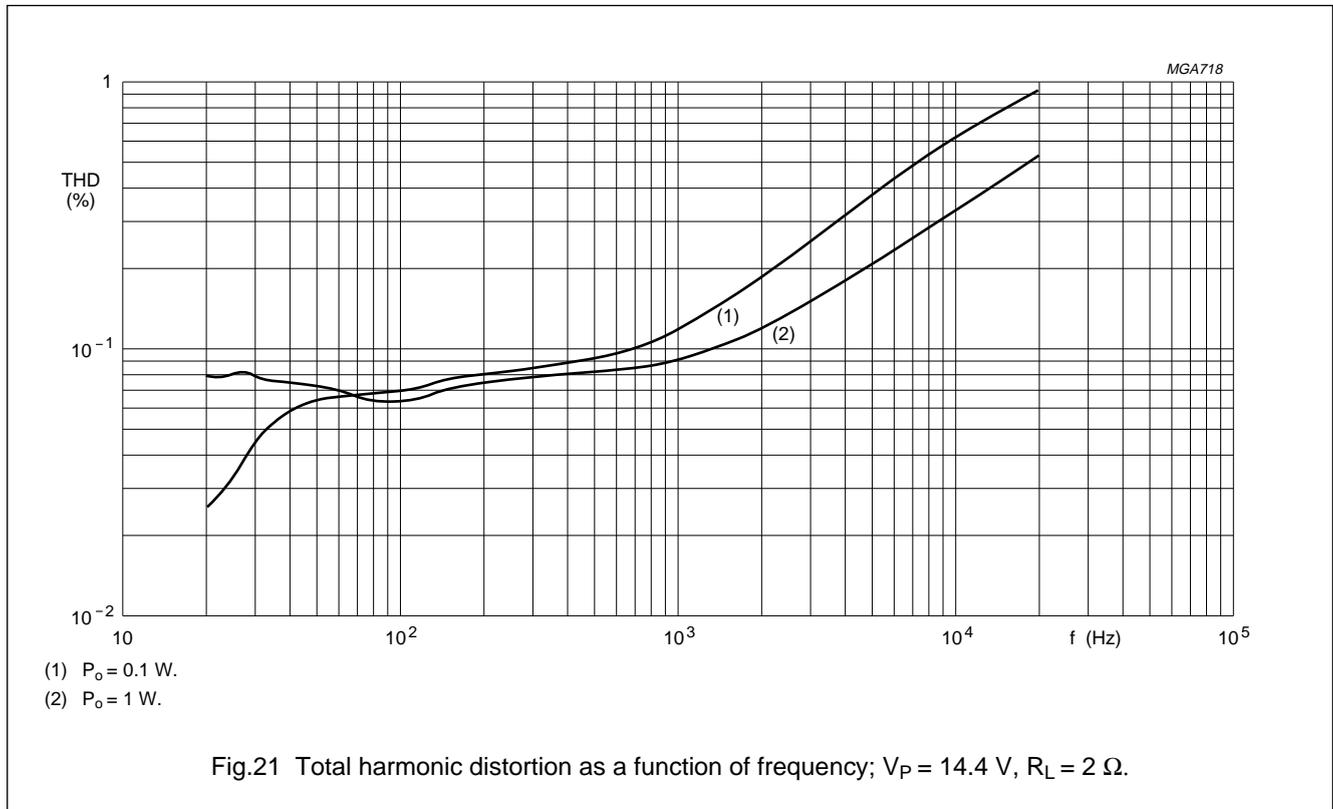
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BTL APPLICATION

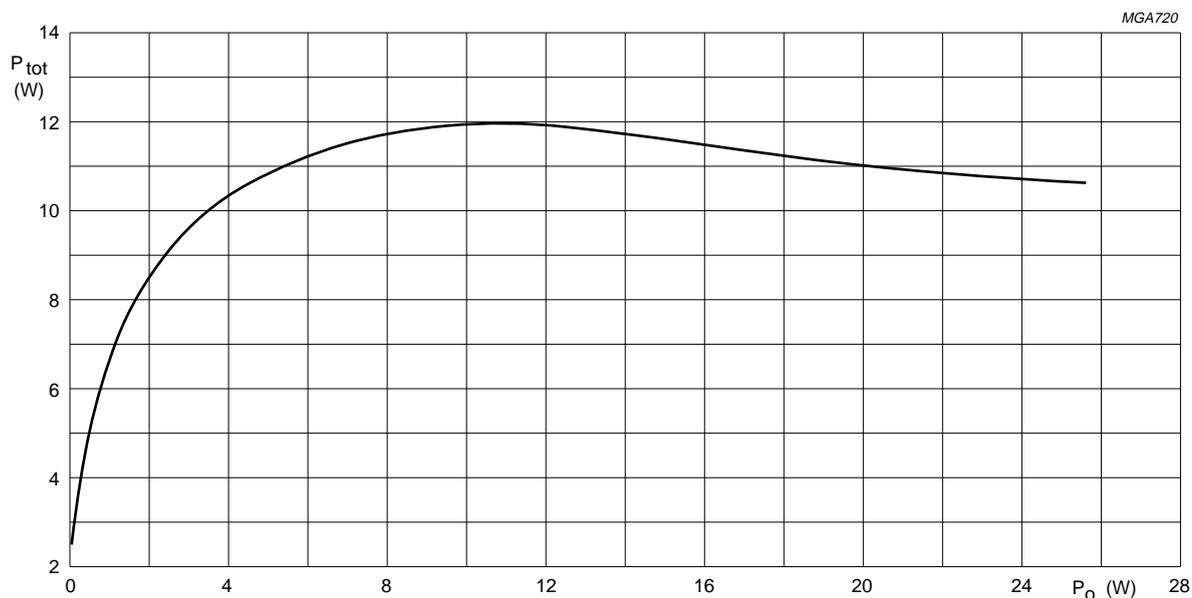


Fig.23 Total power dissipation as a function of output power; $V_P = 14.4$ V, $R_L = 4 \Omega$ (1 channel driven BTL or 4 channels in single-ended mode).

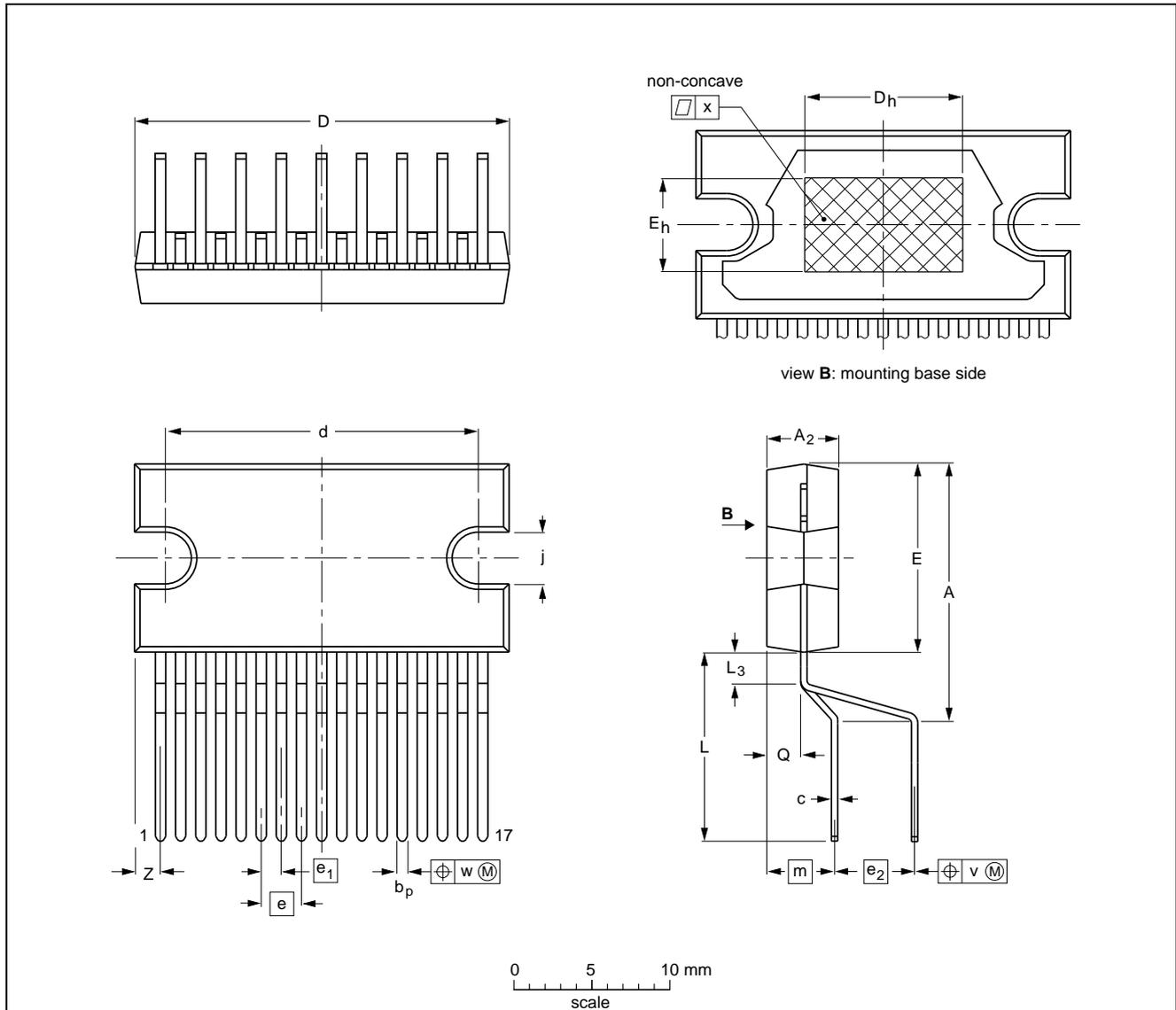
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PACKAGE OUTLINE

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)

SOT243-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	z ⁽¹⁾
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT243-1						92-11-17 95-03-11

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.